Application Note

V25-850C
28Gbit/s VCSEL Reliability Report

Vertically Integrated Systems

Introduction

VI Systems GmbH has a long history of designing superior highspeed VCSELs, which are different from standard commercially available material in terms of bandwidth and energy efficiency.

In order to meet the high reliability standards for Telecom and Datacom applications such as a guaranteed useful lifetime of more than 15 years with a random failure rate of less than 200 FIT (Failures In Time), the basic design has been adapted to allow for much higher bandwidth with limited current and power densities compared to traditional 850nm VCSEL designs. In general this means that the "Time to 1% Failure" must be larger than 100'000 hours in the typical use case as well as the device wear-out with increasing failure rates shall start well after the useful lifetime.

This report summarizes the results of more than three years of reliability studies of 850nm VCSELs produced by VI Systems GmbH to meet performance requirements for direct modulation speeds of more than 25 Gbps.

A typical general device failure probability over time is evolving in a bathtub–like scheme, which distinguishes an initial period of higher early failure rates followed by a floor of random device failures during the useful lifetime and an increasing failure rate due to wear-out mechanisms after the useful lifetime.

Reliability testing and methodology

A basic description for developing acceleration models for electronic components is published e.g. in the Standard JESD91A of the JEDEC Solid State Technology Association.

The upper limit of constant failure rate in time (FIT) is the inverse Mean Time to Failure (MTTF) scaled by one billion device hours and can be calculated using a Chi Square distribution function:

$$\lambda_{average} = X^2_{CL}(2*r+2))*10^9 / (2*n*t_{stress} *AF) \qquad (1)$$

with CL is the Confidence Level (typ. 60%), r gives the number of device failures, n is the sample size, t_{stress} the stress duration and AF is the acceleration factor (if no failure occurs, the function $X^2_{0.6}(2)/2$ yields ~0.92).

For VCSEL the main aging factors are temperature and current density. The acceleration factor AF for the aging of VCSEL is

$$AF = (J_{stress}/J_{use})^N * \exp[E_a/k_B*(1/T_{use} - 1/T_{stress})] \qquad (2)$$

with J_{stress} is the accelerated stress current density, J_{use} is the use current density, T_{use} and T_{stress} are the VCSEL temperatures under use and stress conditions, respectively. k_B is the Boltzmann`s constant. The values of the exponent N and the activation energy E_a had been experimentally determined at current densities <10kA/cm^2 and verified for VCSEL by several groups to be about E_a = 0.7eV and N=2. Opposite to the range of low current densities the degradation at current densities above 20kA/cm^2 occurs much faster with current density. The parameter N increases to ~10 due to the higher

probability of multiple nonequilibrium electrons-holes pairs to recombine nonradiatively at a defect with the growing importance of high-order process of defect generation and growth.

For accelerated aging the devices are powered with a stress current which is significantly higher than the operational current in combination with a stress temperature which is significantly higher than the average temperature during VCSEL operation. With these conditions device failures occur in a reasonable time and the expected lifetime can be predicted by the formulas above.

Failure criterion

As a failure criterion a drift in power by more than 20% (1dB) after the aging time is defined. This is more strict than the usual 2dB drift criterion of commercially available devices, but it shall ensure that strict power budgets are kept for ultra-high speed links.

Device operation for accelerated aging

A typical accelerated aging is performed by applying a set of various stress groups of different currents and temperatures each to a number of comparable devices. For each temperature and current the total number of the chips per identical stress was 60 in three blocks according to three different burn-in conditions prior to the aging study. The aging parameters were selected as:

- 3 temperatures (90, 120, 150°C) to allow extrapolations of the temperature aging coefficients at the same current
- 3 current densities (18kA/cm^2, 25kA/cm^2, 32.4 kA/cm^2 at each temperature) to allow extrapolations of the current trends at fixed temperatures.

As minimum aging current 5mA is chosen, which equals to a current density of 18kA/cm^2 .
The details are given in matrix :

Drive current	Temperature	Temperature	Temperature
	90°C	120°C	150°C
5mA	20x3	20x3	20x3
7mA	20x3	20x3	20x3
9mA	20x3	20x3	20x3

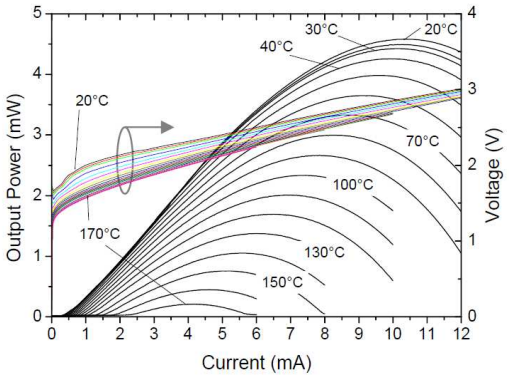
Table 1: Matrix of different aging groups

For each burn-in group a full matrix set of devices is applied for accelerated aging. Altogether there are 540 devices tested with additional 30 devices as sleepers (reference devices, which are only measured, but not operated during application of the stress conditions).

For the actual operation, three stress boards are used in the study for 90°C, 120°C and 150°C respectively. Each board allows aging for roughly 200 VCSELs at three different currents and holding "Sleepers" without current injection.

Device measurements

In **Figure** *1* the typical relation of output power to operation current for several temperatures.



(d)

Figure 1: VCSEL design (a) and optical microscopy images (b, c). (d) LIV curves at different temperatures of a chip with 6 μm aperture.

The data acquisition is taken initially after burn in, then after each 100h, then after each 200h and with 400h. During each read out the chips were cooled to room temperature (25°C) so that the measurements could be done in a comparable way.

Burn-in test results

Very high burn in currents (>35kA/cm^2) cause chip degradation to 20% power level within 10-20 hours. The systematic result of the burn in at high currents is ~3% increase in the power as compared to the level before aging. Ideal burn-in conditions are found to be 8mA at 95°C.

Calculation of Acceleration parameters

To define the parameters for Eq. 2 dependencies of the time to 1% failure versus temperature and current density are to be defined. As the degradation of the power in the initial phase (~20% drop) occurs linearly with time, a percentage of the chips versus aging time dependence can be constructed (**Figure** *2*).

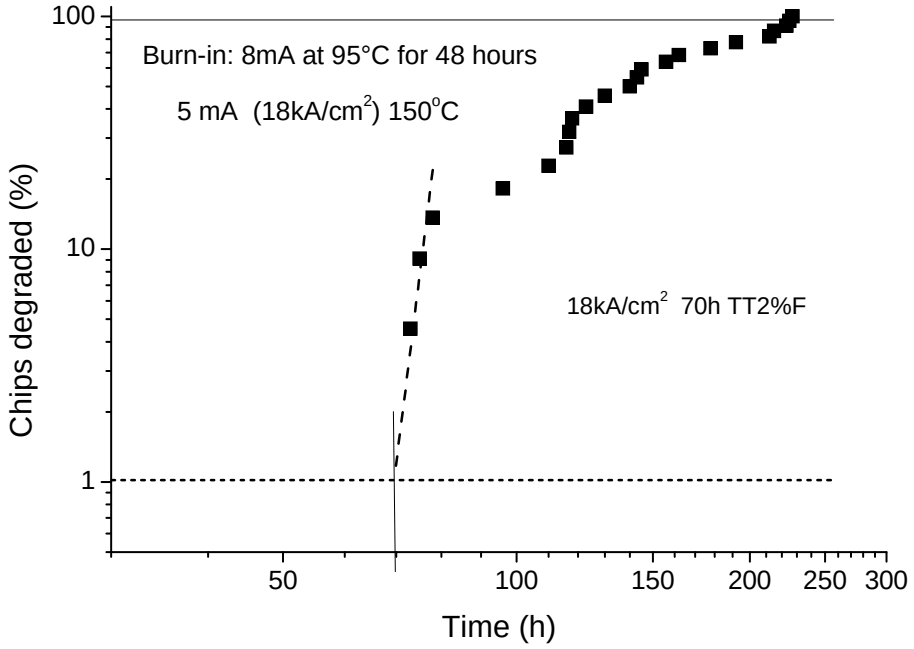


Figure 2. Aging of the chips at 150°C at 18kA/cm^2: Output power at 5mA at room temperature after ageing is measured. The failure criterion is 20% drop in power. Time to 1% failure can be defined from the dependence. No burn-in preselection is applied.

Less extreme conditions are leading only to a slight degradation. In this case longer stress times (up to 1500 hours) and partly also extrapolation has been used to derive the Time to 1% failure.

Figure 3 shows the data at 90°C:

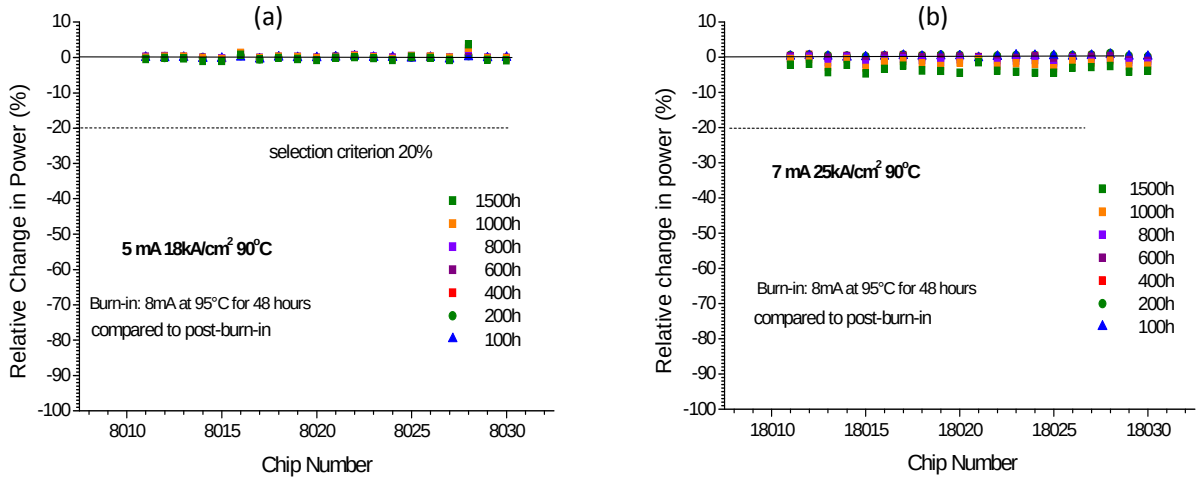


Figure 3. (a) Aging of the chips at 90°C at 18kA/cm^2 and (b) 25kA/cm^2 . No burn-in pre-selection.

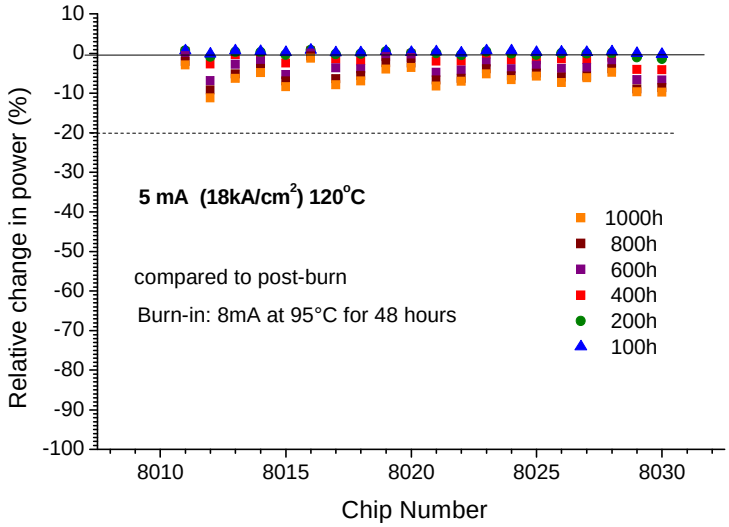


Figure 4. Aging of the chips at 120°C at 18kA/cm$^{2.}$ No burn-in preselection.

Figure 4 shows the power drift distribution over time for operation at normal operation current but elevated temperature of 120°C. One clearly observes the linear drift over time, which is typically related to constant accumulation of defects over time.

Catastrophic random defects ("sudden death"), which can be caused by dislocation growth in GaAs, e.g. as a consequence of ESD or other process or handling related damage has not been observed in any of the stress groups. Those defects would contribute to an increasing random failure rate during

the useful lifetime (this means the drift of optical power due to systematic defect accumulation has not yet reached the 20% failure limit, but the device is suddenly degrading very fast due to a different failure cause.

Long-term monitoring

Additionally a long-term monitoring test has been started, which is close to the actual use conditions. Data for 6000h at 95°C and 5mA (18kA/cm^2) are shown in **Figure** 5.

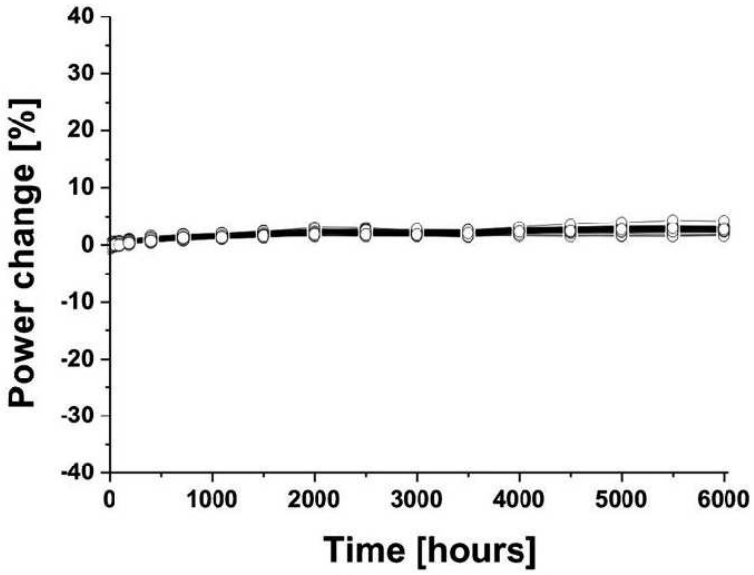
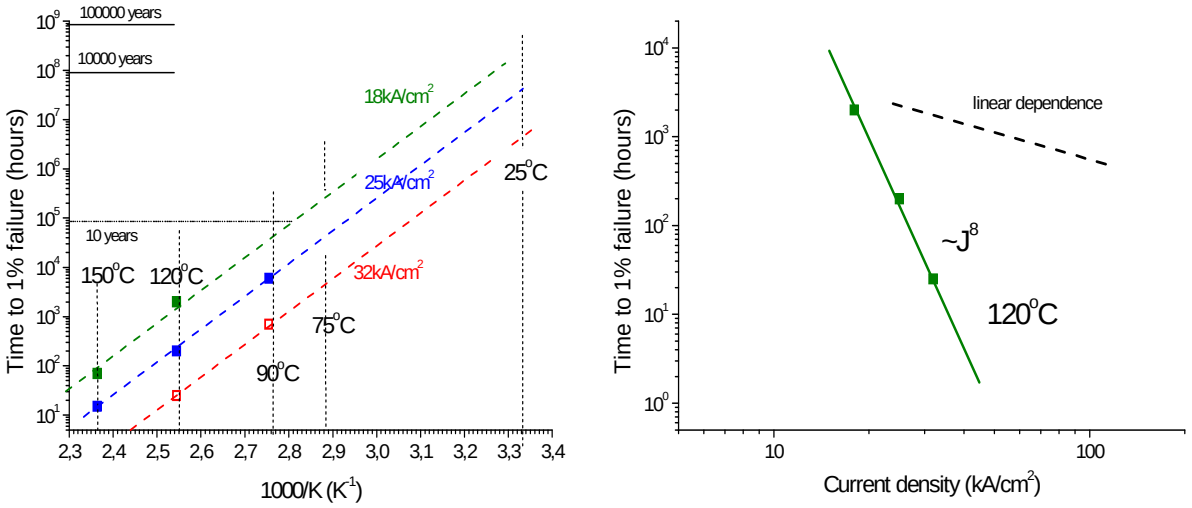


Figure 5: No decrease in the output power of 6 μm aperture VIS 25G VCSEL is found for the accelerated aging time of 6000h at 95°C at 18 kA/cm^2.

Fitting the acceleration model

On the basis of similar charts 1%TTF values at different aging conditions can be extracted or extrapolated assuming a similar power decrease rate. A summary of the results is presented in ***Figure** 6*



(a) (b)

Figure 6. (a) 1%TTF for the VCSEL chips as a function of temperature at different current densities. (b) 1%TTF for the VCSEL chips as a function of the current density for aging at 120°C. The longest test for aging at ~95°C is 6000h at 18kA/cm^2 as shown by the green dotted line. No noticeable degradation was found in agreement with the expected lifetime at this temperature and current. 18kA/cm^2 is enough for 28Gb/s at 85°C at ~-10dBm received power.

The derived parameters based on the 120°C curves for N and all remaining points for E_A are for the power number of current acceleration N=8 and for the thermal activation energy E_A=1.3eV.

The actually derived acceleration equation for Drift of optical power (wear-out) is given by:
$AF = (J_{stress}/J_{use})^8 \exp[(1.3eV)/k_B*(1/T_{use} - 1/T_{stress})]$

Given the homogenous and systematic decrease in optical power due to the observed wear-out effects under accelerated stress conditions, the 1%TTF value can be seen as a very conservative approach to estimate the useful lifetime of the device under certain operation conditions. It can directly be referenced from Figure 6 (a).

Results and conclusions

For the systematic drift of optical output power (wear-out), we could derive an acceleration model, which supports extrapolation of useful lifetime as a function of stress conditions in a systematic matter (chapter 5.1). This is to be differentiated from random failure rates (FIT or MTTF).

Useful Lifetime and wear-out

The most important task first, is to guarantee that the design of High Speed VCSELs can manage to systematically sustain the material wear-out due to temperature and current induced aging effects during their reasonable useful lifetime.

In this case, the distribution of the drift was very homogenous and strongly accelerated with both current density (to the power of eight) and temperature (having a thermal Activation Energy of 1.3eV).

This suggests for operation at a typical current of I=5mA or current density of J=18kA/cm2 and 45°C operation temperature a Mean Time to Failure (MTTF) of approximately 114 Mio hours, or a Time to 1% failure of more than 2 Mio hours. In this case the useful lifetime will be between the two values and not limiting the operation time.

Even at 90°C and 5mA operation a MTTF value of more than 35 years can be determined.

Estimation of an upper limit for Random Failure Rates

Due to the limited number of devices, the random failure rates can not be assumed to be zero, even if no sudden death event has been observed.

Also the acceleration parameters are not necessarily the same as for wear out. For acceleration, the recommended conservative default values according to Telcordia GR-468–Core have been used:

$AF = (J_{stress}/J_{use})^2 \exp[(0.35eV)/k_B*(1/T_{use} - 1/T_{stress})]$ With those values we have collected in total more than 4.8 Mio device hours within all groups, referenced to the normalized operation conditions of 45°C ambient temperature and 5mA operation current.

Given a confidence level of 60%, we can derive an upper limit of the random FIT rate of 189.

In order to get sufficient data we included both the 8mA as well as the 10mA burn-in group for evaluation of random failures. The failure criterion is sudden death, which means a sudden drop in optical power of more than 90% between two readouts. The readout time has been limited to a number, that systematic drift was not preventing the evaluation.

Conclusions

As a conclusion it can be observed that for operation at usual operation conditions of 45°C and 18kA/cm ^ 2 the systematic lifetime is virtually infinite.

In case of constant operation at elevated temperatures (e.g. in uncooled, compact environments), we still can derive reasonable useful lifetimes with MTTF values of more than 35 years for ambient (heatsink) temperatures of up to 90°C.

The maximum burn-in conditions are found to be 90°C and 8mA.

After a period of 48hrs of burn-in under this condition, an upper limit of the **random failure rate of less than 189 FIT at 60% confidence leve**l can be derived from the current results. However the results are still limited by statistics, since no random failure event happened. Thus it can be assumed, that the real FIT rate is even lower.