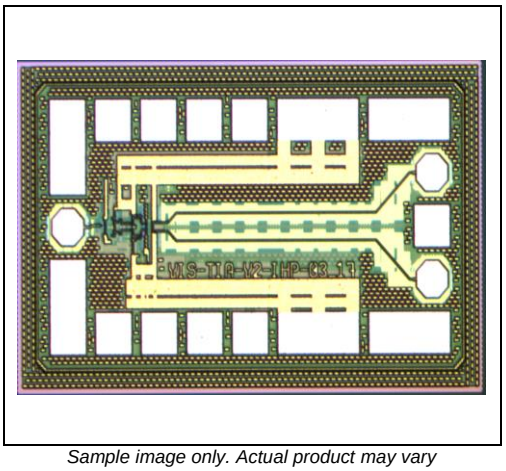
Datasheet

T56-150C

Vertically Integrated Systems

Transimpedance Amplifier 56 Gbit/s



Sample image only. Actual product may vary

Product Code: T56-150C

Preliminary

Product Description

The T56-150C is a high speed transimpedance amplifier (TIA) IC designed for use by 56G receiver modules in fiber optic transmission systems. The T56-150 operates from a single +3.3 V supply typically dissipating 150 mW of DC power and is designed for the use with PIN photodetectors in a wire-bond or flip-chip design.

The IC has a single-ended input (In) and a differential output (Out+, Out-). It includes the cathode connection for the photodiode (Cath) as well as a bias path through the internal pin (PD). The TIA features input/output DC-offset cancellation and is also equipped with gain control functionality which can be adjusted through the analog pin (Vmod).

Features

- 0.25 µm SiGe-BiCMOS technolgy
- Supports data rates of up to 56 Gbit/s
- Low power consumption: typ. 150mW
- Differential Output 100 Ω
- 3.3V power supply
- Small dimensions 1040 µm x 640 µm

Applications

- CEI-56G
- Fiber optics systems tests
- Research and development

Parameter	Typical (PD chips)	Notes
Data rate	Up to 56 Gbit/s	
Supply Voltage (V_{CC})	3.3 V	
Power dissipation	150 mW	
Differential output resistance	100 Ω	
Ambient Operating Temperature	-5 to +85°C	

Simplified Block Diagram

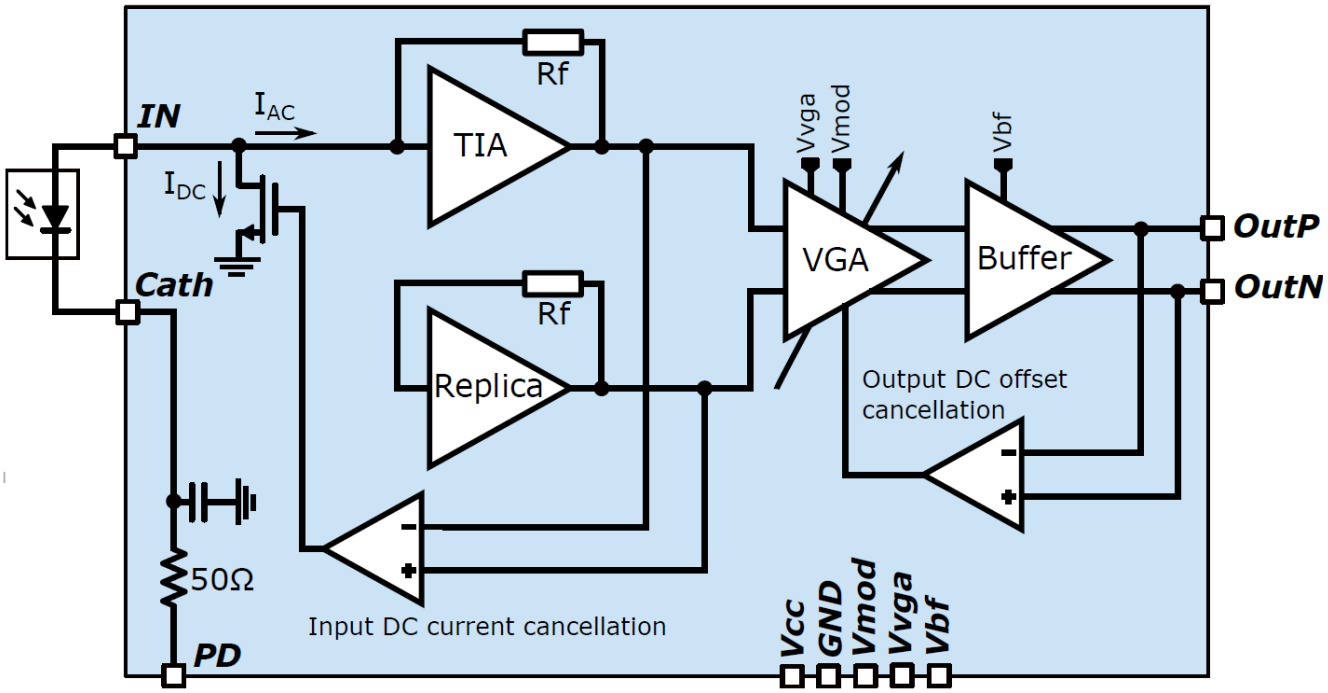


Figure 1. Simplified block diagram of the IC

The block diagram of the T56-150 is shown in Figure 1. It consists of three stages: an input transimpedance stage (TIA), a variable gain amplifier (VGA) and a 50Ω output buffer. The IC has single-ended input (IN) and differential output (OutP OutN). A replica TIA provides the VGA with DC-balanced inputs. A bias path for the photodiode is provided on-chip through the pin (PD) and cathode (Cath) that includes a low pass filter in order to damp eventual oscillations. The IC is operated with 3.3 V supply (VCC and GND) and equipped with various analog control pins (Vmod, Vvga, Vbf). Vmod defines the gain of the VGAand Vvga and Vbf serve to control the biasing currents of the VGA and output buffer stages, respectively. In typical operation Vvga and Vbf should be connected to Vcc; control on these parameters allows for optimization to accommodate deviations in the load characteristics or assembly tolerances.

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Pad Layout

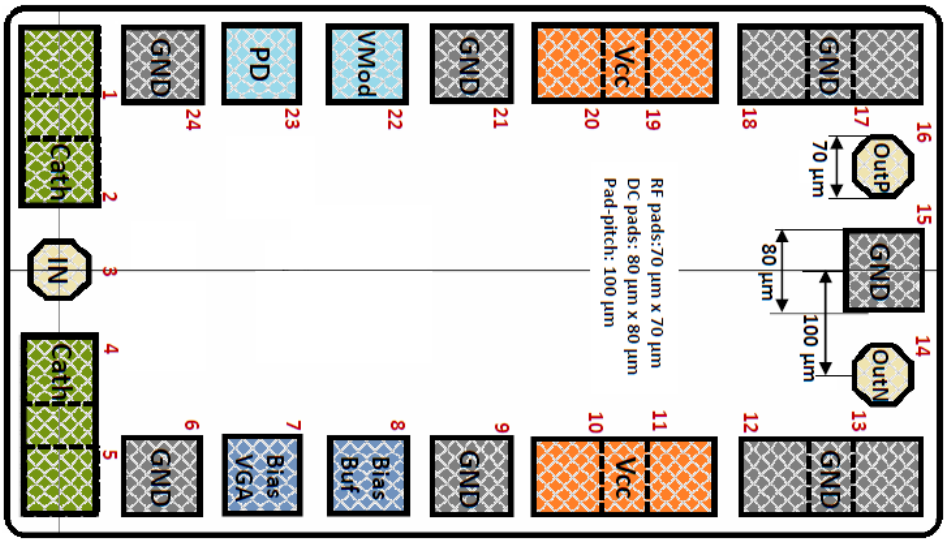

Figure 2. Pad layout of the IC

Pad description

Name	Pin	Symbol	Description	Function
In	3	IN	Input current (to PD anode)	
Out+	16	OutP	HF output voltage (positive)	
Out-	14	OutN	HF output voltage (negative)	
Vcc	10,11,19,20	Vcc	Supply voltage	
GND	6,9,12,13,15,17,18,21,24	GND	Ground	
PD	23	PD	Photodiode bias	
Vmod	22	Vmod	VGA gain control	
Vbuf	8	Vbf	Control Buffer biasing current (1mA)	
Vvga	7	Vvga	Control VGA) biasing current (1mA)	
Cathode	1,2,4,5	Cath	Photodiode cathode	

Control Voltages Description

Vcc
Power supply of the IC.

PD
Control voltage PD defines the reverse bias of the photodiode. This voltage is applied through an on-chip bias path that serves to damp eventual oscillations caused by the packaging parasitics.

Cath
Photodiode cathode.

Vmod
Control voltage Vmod defines the VGA gain. It can be tuned between 1.1V (low gain setting) and 3.3V (high-gain setting), providing ~15dB gain control range. Differential S21 parameter change with Vmod is displayed in Fig. 3.

Vbuf
Control voltage Vbuf defines the biasing current for the output buffer. In typical conditions it should be connected to Vcc. If control on this parameter is desired, it can be tuned between 3V and 3.5V, mainly affecting the output voltage swing.

Vvga
Control voltage Vvga defines the biasing current for the VGA. In typical conditions it should be connected to Vcc. If control on this parameter is desired, it can be tuned between 3V and 3.5V mainly affecting the bandwidth and eye jitter.

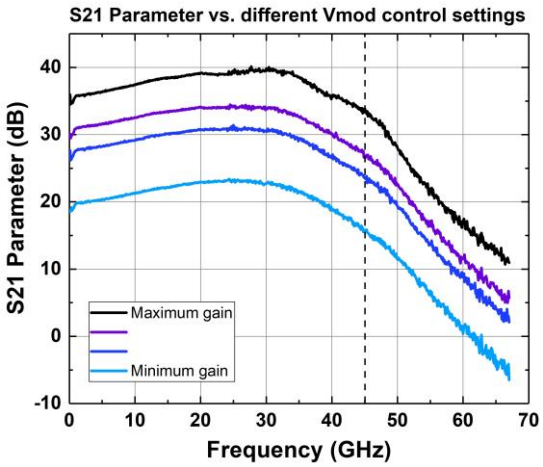

Figure 3. Influence of the Vmod control voltage on the S21 parameter

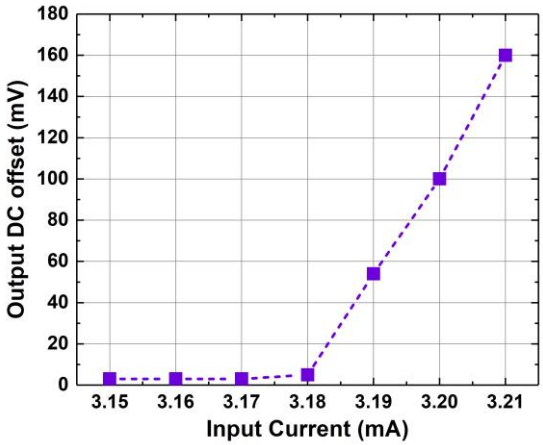

Figure 4. Influence of the input DC current on the dc offset of the output signal

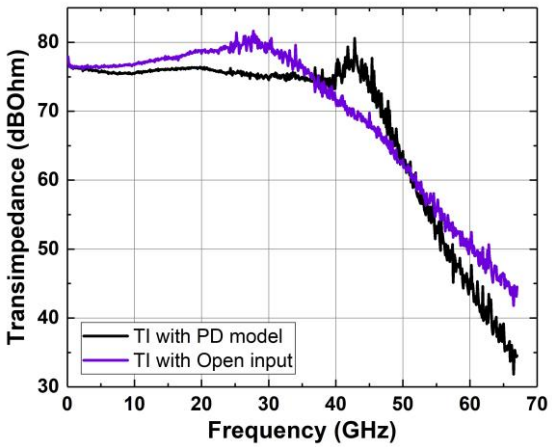

Figure 5. Measured differential transimpedance gain taking into effect the load characteristics.

Turn on conditions

To properly switch on the IC, Vbuf and Vvga supplies should be provided before Vcc, if they are not connected to Vcc (as recommended in typical operation). Vmod control can be applied simultaneously with or later than Vcc.

Operating conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current (DC)			0.2		3	mApp
Input current (AC)			0		1.2	mA
Supply voltage	V_{cc}			3.3		V
VGA gain control	V_{mod}		1.1		3.3	V
Control buffer biasing current (1mA)	V_{bf}		3	3.3	3.5	V
Control VGA biasing current (1mA)	V_{vga}		3	3.3	3.5	V
Photodiode bias	PD			5	5	V
Bondwire inductance for signal pins				250	400	pH
Bondwire inductance for cathode		multiple		4 x 250	4 x 400	pH

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features ESD protection, devices subjected to ESD stress may lose in performance and functionality.

Quality of the input signals should be monitored and supplied based on test circuit (Fig …)

Test circuit

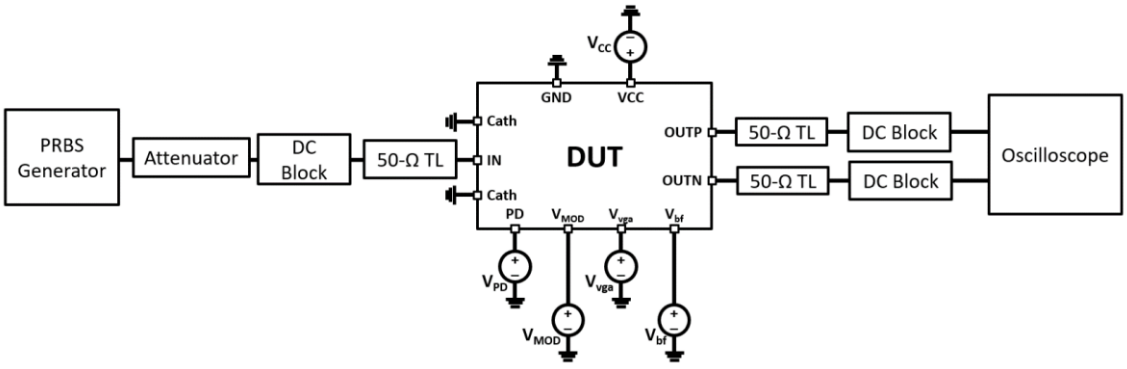

Figure 6. Test circuit

The functionality of the IC can be monitored and operated based on test circuit (Fig. 6)

300 pF external capacitor recommended to clean the Vcc DC signal.

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current (DC)					3	mApp
Input current (AC)					1.8	mA
Power supply voltage	V_{cc}	w/ respect to GND	-0.5		3.5	V
Vbuf, Vvga, Vmod	V_{buf} V_{VGA} V_{mod}	w/ respect to GND	0		3.5	V
Soldering temp		<10 sec			+300	°C
Operating temperature	T_{OP}		-5		+85	°C
Vcontrol currents (Vvga, Vbuf, Vmod)					2	mA

Characteristics & output parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Data Rate				50	56	Gb/s
Differential output voltage				800		mVpp
Differential transimpedance gain			1		6.5	KΩ
S21 Bandwidth*				45		GHz
|S22|Output return loss		< 45GHz	20		8	dB
Input referred integrated noise*		45 GHz		13.2		pA/sqrt(Hz)
Rise/Fall time		20-80%		12	15	
Power dissipation			120	150	180	mW

* The bandwidth is stated for a 50 Ω load. The bandwidth is higher with a photo-diode, see Fig. 5.
* Integrated noise is calculated as following from the measurement (0.65mVrms is the noise of the oscilloscope module itself)

- $I_{n,in} = \frac{\sqrt{(9.2\ mV)^2 - (0.65mV)^2}}{3300} = 2.78\ \mu A_{rms}$
- $I_{n,in,avg} = \frac{I_{n,in}}{\sqrt{45\ GHz}} = 13.2\ pA/\sqrt{Hz}$

Performance

Electrical measurements were performed on a 50 Ω load. Improvement of the electrical characteristics is expected in assembly with a photo-diode chip. The performance of the assembly strongly depends on the model of the optoelectronic device and assembly scheme.

Eye diagram at 56 Gbit/s (electrical)

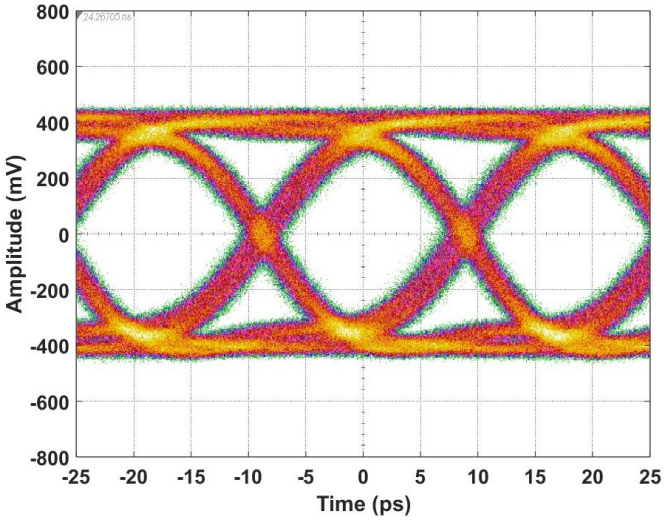

Figure 7. Differential Electrical eye-diagram at 56 Gbit/s bit rate. Input signal: 54mVpp

S-Parameters

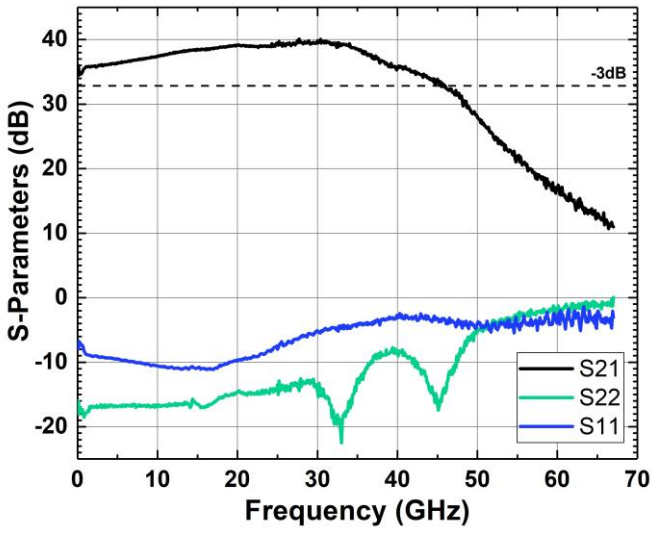

Figure 8. S21, S22 and S11 parameters measured on the IC

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Mechanical dimensions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Die width	W			1.04		mm
Die length	L			0.64		mm
Die thickness	H			200		µm
DC square pad dimensions				80		µm
RF octagonal pad dimensions				70		µm
Pad pitch				100		µm

Limited Qualification Notification

The T56-150C has been tested to meet specifications outlined in this data sheet at room temperature. However, it has not undergone full qualification testing or characterization and therefore may not meet the performance specifications over all extremes.

RoHS Compliant

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